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Filing Date	August 14, 2000
First Named Inventor	Paul A. Farrar
Art Unit	2811
Examiner Name	N. Parekh
Attorney Docket Number	M4065.0082/P082-A

Total Number of Pages in This Submission

ENCLOSURES (*Check all that apply*)

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
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- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
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- [ ] Proprietary Information
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- [x] Other Enclosure(s) (please identify below):

Request for Reinstatement of Appeal; Appellant's Supplemental Appeal Brief

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP Thomas J. D'Amico
Signature	
Date	April 15, 2004

Docket No.: M4065.0082/P082-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Paul A. Farrar

Application No.: 09/638,026

Filed: August 14, 2000 Art Unit: 2811

For: METHOD OF FORMING A MICRO SOLDER BALL FOR USE IN C4 BONDING PROCESS Examiner: N. Parekh

REQUEST FOR REINSTATEMENT OF APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action mailed January 15, 2004 reopening prosecution of the above-captioned matter in response to Appellant's Brief filed November 6, 2003, Appellant hereby requests that the Appeal be reinstated, pursuant to 37 C.F.R. § 1.193(b)(2). Appellant's Supplemental Appeal Brief is filed herewith.

Dated: April 15, 2004

Respectfully submitted,

By 

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Docket No.: M4065.0082/P082-A
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Paul A. Farrar

Application No.: 09/638,026 | Confirmation No.: 8833

Filed: August 14, 2000 | Art Unit: 2811

For: METHOD OF FORMING A MICRO SOLDER BALL FOR USE IN C4 BONDING PROCESS | Examiner: N. Parekh

APPELLANT'S SUPPLEMENTAL APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a Reinstated Appeal pursuant to 35 U.S.C. § 134 and 37 C.F.R. §§ 1.191 et seq. from the rejection of claims 40, 43-51, 68-72, and 74-75 of the above-identified application mailed on January 15, 2004, and in furtherance of the Notice of Appeal, filed in this case on August 18, 2003 in response to the April 17, 2003 Final Rejection.

The fees required under § 1.17(f) were previously paid with the November 6, 2003 filing of Appellant's original Appeal Brief. Any deficiency in the fees associated with the brief should be charged to Deposit Account No. 04-1073. This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

Appellant hereby incorporates by reference the November 6, 2003 Appeal Brief, the substance of which is largely reproduced below. Appellant's Supplemental Appeal Brief sets forth, at Parts VIII(E)-(F) below, arguments against Examiner's new grounds for the rejections of claims 69 and 70. Additionally, Part VIII(A) has been supplemented over the November 6, 2003 version. Previous references to the April 17, 2003 Final Rejection have been amended to refer to the January 15, 2004 Office Action.

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Micron Technology, Inc., the assignee of this patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, his legal representative, or the assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 17 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 1-39 , 41-42, 52-67, and 73.

2. Claims withdrawn from consideration but not canceled: none.

3. Claims pending: 40, 43-51, 68-72, and 74-75.

4. Claims allowed: none.

5. Claims rejected: 40, 43-51, 68-72, and 74-75.

C. Claims On Appeal

The claims on appeal are claims 40, 43-51, 68-72, and 74-75.

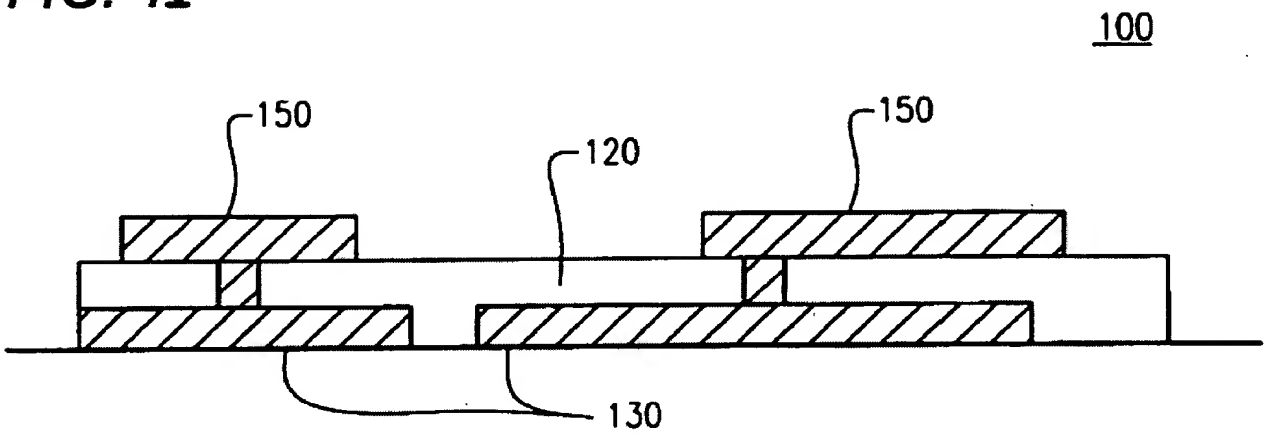
IV. STATUS OF AMENDMENTS

There have been no amendments subsequent to the April 17, 2003 Final Rejection.

V. SUMMARY OF INVENTION

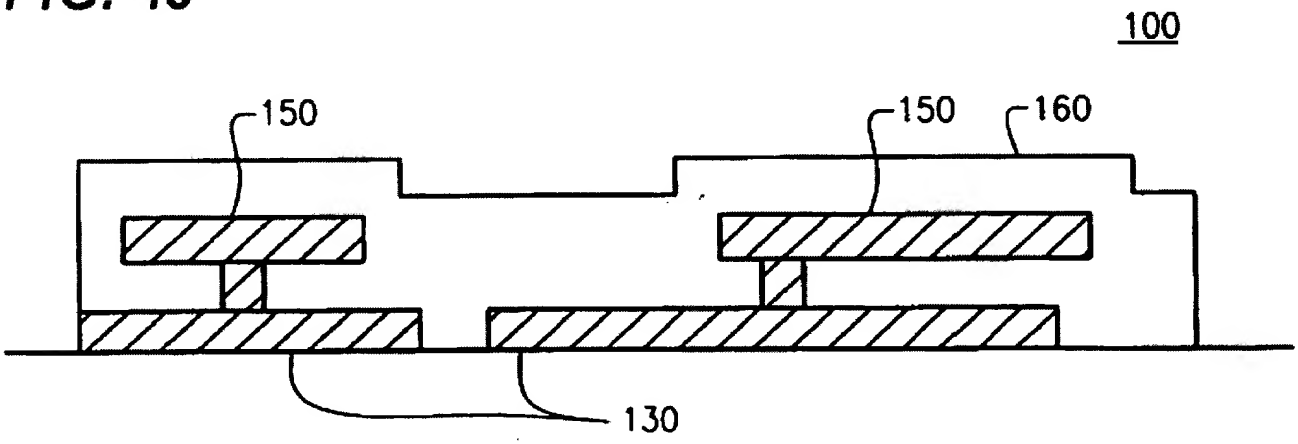
The present invention relates to a semiconductor device having an improved connector structure including small solder contacts. Semiconductor device 100 of the present invention shown in Fig 4I, reproduced below, comprises a metal contact 130 and a first insulating layer 120 overlying metal contact 130. See page 6, line 26 – page 7, line 1 of the specification. Semiconductor device 100 further comprises metal pad 150 overlying first insulating layer 120 and in contact with metal contact 130. See page 7, lines 18 – 22; page 8, lines 26 – 29 of the specification.

FIG. 4I



Referring to Fig. 4J, reproduced below, semiconductor device 100 also comprises a second insulating layer 160 formed over metal pad 150. See page 9, lines 1 – 2 of the specification.

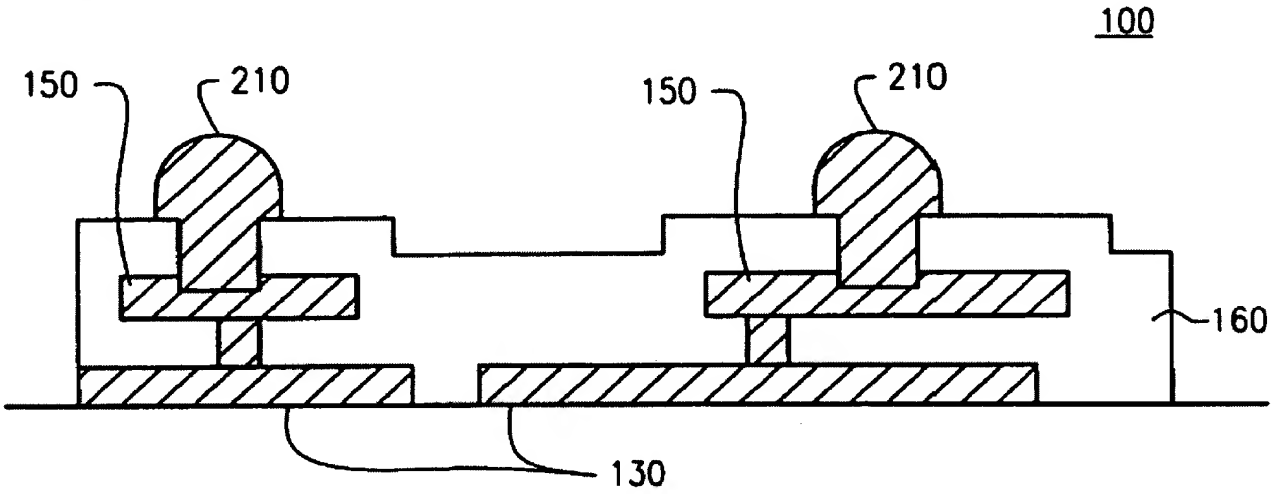
FIG. 4J



As shown in Fig. 4P, reproduced below, semiconductor device 100 of the present invention also comprises at least one solder contact 210 formed in second insulator 160 and in contact with metal pad 150. See page 10, lines 13 – 19 of the

specification. Solder contact 210 provided in the present invention has a diameter of less than 100 μm. See page 11, lines 20 – 27 of the specification.

FIG. 4P



The present invention also relates to semiconductor devices 100 as shown in Fig. 4P above, with solder contacts 210 having a diameter of less than 50 μm, less than 25 μm, or less than 10 μm. See page 11, lines 20 – 27 of the specification. The present invention also relates to a semiconductor device 100 as shown in Fig. 4P where solder contact has a diameter of approximately 2 μm. See id.; page 11, lines 18 – 19 of the specification.

These semiconductor devices having solder contacts which are smaller and can be more densely fabricated on an integrated circuit package than prior solder contacts are favorable because of the benefit that a greater number of smaller solder contacts may be included for a given integrated circuit package area, providing a greater number and density of I/O terminals. See page 4, lines 17 – 23 of the specification. Prior to Appellant's development of the present invention, no one had created a semiconductor device having solder contacts with a diameter of less than 100 microns. Appellant discovered a unique way to manufacture such small solder

contacts using the tape liftoff process described in the specification. See page 6, line 26 – page 10, line 20 of the specification. As of the time of the application's filing, Appellant was not aware of any other semiconductor device successfully integrating solder contacts of the claimed size. As will be described below, the January 15, 2004 Office Action contains no evidence that such a semiconductor device, or effective method of making it, had been taught or suggested prior to the filing date of the present application.

VI. ISSUES

A. Should the rejection of claims 40, 43-49, 68, 71-72, and 74-75 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,925,931 to Yamamoto (hereinafter "Yamamoto") in view of U.S. Patent No. 6,249,347 to Svetkoff et al. (hereinafter "Svetkoff") be reversed?

B. Should the rejection of claims 50-51 under 35 U.S.C. § 103 as being unpatentable over Yamamoto in view of Svetkoff as applied to claim 40 and in further view of the admitted prior art be reversed?

C. Should the rejection of claim 69 under 35 U.S.C. § 103 as being unpatentable over Yamamoto and Svetkoff as applied to claim 40 and in further view of U.S. Patent No. 5,888,884 to Wojnarowski (hereinafter "Wojnaroski") be reversed?

D. Should the rejection of claim 70 under 35 U.S.C. § 103 as being unpatentable over Yamamoto, Svetkoff, and Wojnarowski as applied to claims 40 and 69 above, and further in view of Japanese Patent No. JP 8—236938 to Takashi et al. (hereinafter "Takashi") be reversed?

VII. GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below:

Group	Claim(s)
I.	Claims 40, 45-51, 68, and 71.
II.	Claims 74-75.
III.	Claim 43.
IV.	Claims 44 and 72.
V.	Claim 69.
VI.	Claim 70.

Claims of Group I stand or fall together. Claims of Group II stand or fall together. Group III includes only one claim. Claims of Group IV stand or fall together. Group V includes only one claim. Group VI includes only one claim. No claim stands or falls together with any claim of a different Group. In Section VIII below, Appellant has included arguments supporting the separate patentability of each claim Group, as required by M.P.E.P. § 1206.

VIII. ARGUMENTS

A. The Subject Matter of Claims 40, 45-51, 68, and 71 Would Not Have Been Obvious Over Yamamoto in View of Svetkoff

Claim 40 recites a semiconductor device comprising: a semiconductor structure having at least one metal contact formed on a surface thereof (represented as metal contact 130 in Fig. 4I, reproduced above); a first insulator layer overlying said at least one metal contact (first insulating layer 120); at least one metal pad overlying said first insulator layer and in contact with said at least one metal contact (metal pad 150); a second insulator layer overlying said at least first one metal pad (second insulating layer 160 in Fig. 4P, reproduced above); and at least one solder contact formed in the

second insulator and in contact with said at least one metal pad, said solder contact having a diameter less than 100 μm (solder contact 210).

Referring to Yamamoto Fig. 7, reproduced below, the Office Action dated January 15, 2004, states that Yamamoto discloses a semiconductor device comprising a metal contact 23 formed on the surface thereof; a first insulator layer 24/41 overlying the metal contact 23; a metal pad 50 overlying the first insulator layer 24/41 and in contact with the metal contact 50; a second insulator layer 47 overlying the metal pad 50; and a solder ball 48 formed in the second insulator layer 47 and in contact with the metal pad 50. January 15, 2004 Office Action, pages 3-4.

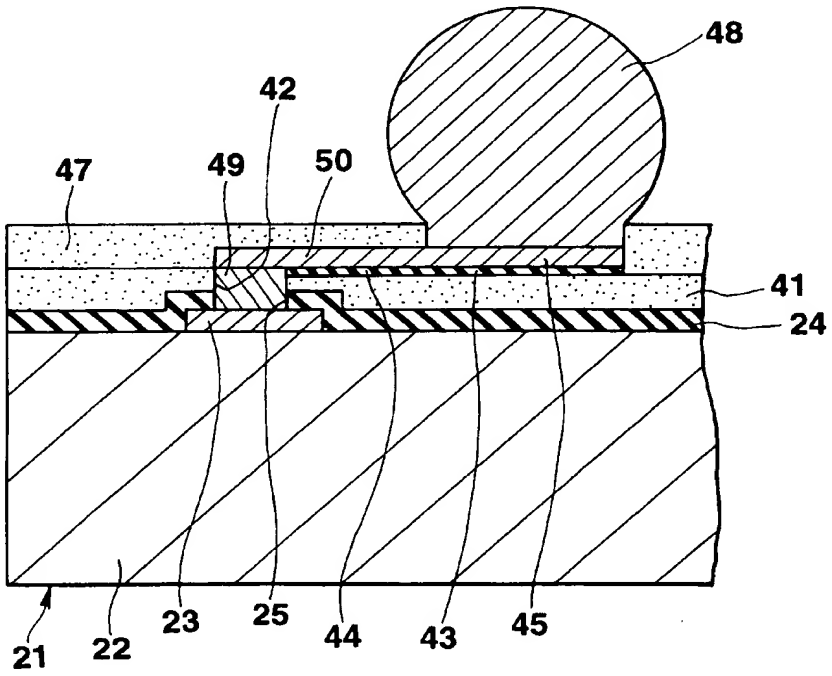


FIG.7

The Office Action correctly concedes that Yamamoto fails to disclose a solder contact 48 having a diameter less than 100μm. Appellant notes that Yamamoto fails to

disclose any particular size for the solder contact utilized in Yamamoto's semiconductor device. Indeed, as noted in the Background of the Invention portion of Appellant's patent application, existing processes at the time of the present invention were incapable of providing solder contacts with a diameter of less than 100 microns. See page 4, lines 17 – 18 of the specification.

Recognizing that Yamamoto does not teach the claimed solder balls, the Office Action turns to Svetkoff for this teaching. However, Svetkoff does not relate to solder contacts and does not include an enabling disclosure for making any solder contacts. Rather, Svetkoff describes a system and method for three-dimensional imaging of "non-cooperative" targets that are typically difficult to measure by optical means due to light reflection, scattering and geometry. Col. 1, lines 59 – 61; col. 5, lines 2 – 5.

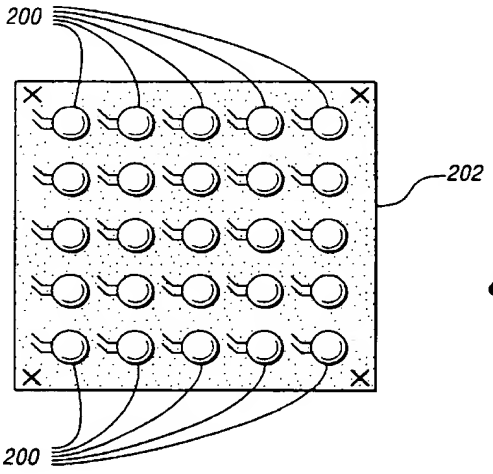


Fig. 11

The Office Action argues that because Svetkoff mentions (as a type of non-cooperative target that may be studied using the Svetkoff system) "a miniature/micro ball grid array (BGA) device using solder balls ... having a typical range of 10-300 microns [element 200 shown in Fig. 11, reproduced above] to achieve the increased

interconnect density and very fine geometries" that it would have been obvious to employ solder balls of this size in Yamamoto.

Appellant respectfully submits that Svetkoff cannot be combined with the teachings of Yamamoto as the basis for an obviousness rejection under 35 U.S.C. § 103(a) because the Svetkoff imaging system is clearly not analogous to the semiconductor device of the present invention. Appellant further submits that, even if Svetkoff were analogous, it still does not sufficiently teach how to make the imaged solder balls described therein, and therefore the claimed semiconductor device is not rendered obvious from the teachings of Yamamoto in view of Svetkoff.

1. Svetkoff is not Analogous Art to the Field of the Present Invention and Therefore may not be Combined with Yamamoto

"In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." In re Oetiker, 977 F.2d 1443, 1446 (Fed. Cir. 1992); M.P.E.P. § 2141.01(a). A reference is "reasonably pertinent" if, "even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem." In re Clay, 966 F.2d 656, 659 (Fed. Cir. 1992).

That Svetkoff does not actually relate to the field of the present invention is clearly illustrated by Svetkoff Fig. 5 and the accompanying text. As stated in Svetkoff:

> Referring specifically to Fig. 5 [reproduced below], an object of the invention is to provide a high speed method and system for measuring a miniature spherical mirror like a solder ball 46 or wafer, mounted on a plane mirror or pad 48 formed on a substrate 50 and producing a very high contrast bump-background image allowing for accurate measurement of

diameter, devoid of occlusion and with minimal reflection noise for many pad backgrounds. Fig. 5 shows a spatial filter 52 through which an incident ray 54 passes and bounces off the ball surface to form reflected rays 56, multiple reflections 58, and specular reflection 60. The spatial filter 52 (i.e. confocal slit) provides the indicated filtering action.

Col. 6, lines 25 – 37.

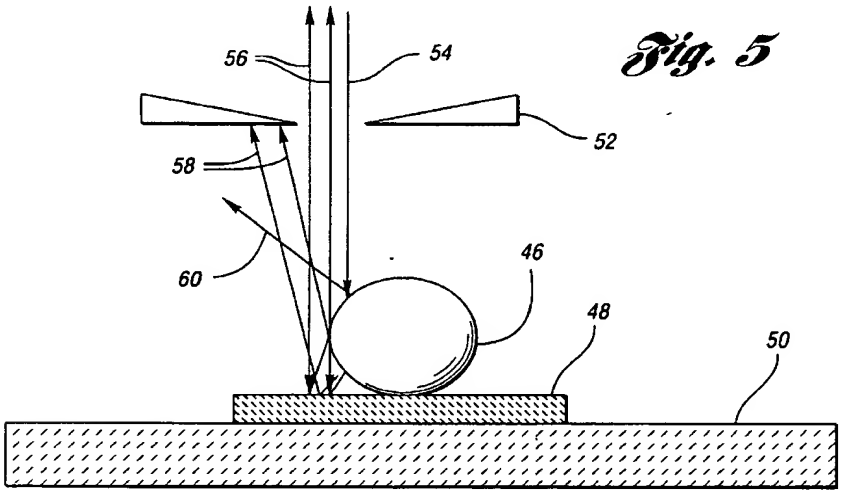


Fig. 5

This is obviously different from the field of the present invention and significantly Svetkoff does not teach how to make a semiconductor device with solder balls in the range of 10-300 microns. Although the Office Action states that Svetkoff teaches a miniature ball grid array of solder balls "having a typical range of 10-300 microns to achieve the increased interconnect density and very fine geometries/ground rules," this is incorrect, as the solder balls mentioned in Svetkoff are not part of the invention therein and are simply given as an example of the size of non-cooperative targets that may be studied by the claimed invention. In other words, Svetkoff does not teach a die having solder balls in the diameter range of 10-300 microns, but that the disclosed optical system would be capable of studying solder balls in that range. There is nothing in Svetkoff to teach or suggest how to make or use a die having solder balls in the range of 10-300 microns.

Since Svetkoff is directed to an imaging system and has no disclosure of how to make a semiconductor device, much less one having solder balls less than 100 microns in diameter, it cannot permissibly be combined with the teachings of Yamamoto to render the claimed invention obvious.

2. Svetkoff does not Provide an Enabling Disclosure of the Mentioned Solder Balls

Even assuming arguendo that Svetkoff is directed to an analogous prior art, Appellant respectfully submits that Svetkoff's disclosure with respect to solder balls is insufficient to teach one of ordinary skill in the art how to make a semiconductor device having solder balls less than 100 microns in diameter. As mentioned above, Svetkoff mentions that his system can image solder balls or bumps 10-300 μm in diameter (col. 11, line 27-37). However, this is merely a bald reference to an example of a microelectronic or micromechanical device which can be studied in Svetkoff, and not an enabling disclosure of a die structure having solder balls 10-300 μm in diameter. Indeed, there is absolutely no disclosure in Svetkoff for making a semiconductor device having solder balls in the disclosed range and certainly no teaching for making a semiconductor device having solder balls less than the claimed 100 microns in diameter.

As the Federal Circuit has stated: "In order to render a claimed apparatus or method obvious, the prior art must enable one skilled in the art to make and use the apparatus or method." Beckman Instruments, Inc. v. LKB Produkter AB, 892 F.2d 1547, 1551, 13 USPQ2d 1301, 1304 (Fed. Cir. 1989) (citing In re Payne, 606 F.2d 303, 314, 203 USPQ 245, 255 (CCPA 1979) ("References relied upon to support a rejection under 35 USC 103 must provide an enabling disclosure, i.e., they must place the claimed invention in the possession of the public. An invention is not 'possessed' absent some known or obvious way to make it.") (quoting In re Hoeksema, 399 F.2d 209, 274

(C.C.P.A. 1968)). The Federal Circuit reiterated this proposition in Motorola Inc. v. Interdigital Technology Corp., 121 F.3d 1461, 1472, 43 USPQ2d 1481, 1489 (Fed. Cir. 1997) (quoting Beckman, supra).

Where the reference does not include an enabling disclosure, "secondary evidence, such as other patents or publications, can be cited to show public possession of the method of making and/or using [the claimed article]." M.P.E.P. § 2121.01(I). Here, there is no such enabling disclosure as the January 15, 2004 Office Action fails to cite any secondary evidence that a method of making and/or using solder balls less than 100 μm in diameter was in the public possession at the time of the present invention. Only Appellant has disclosed a unique tape liftoff process capable of producing solder balls of the size claimed (less that 100 microns) on a die.

Since Yamamoto and Svetkoff (1) are not properly combinable as non-analogous art, and (2) Svetkoff does not provide an enabling disclosure of a device having solder contacts with a diameter less than 100 μm as recited in claim 40, Appellant submits that the rejection of claim 40 and claims 45-51 and 68 dependent therefrom is erroneous. Independent claim 71 recites similar limitations to claim 40 and its rejection is also erroneous for the reasons set forth above.

Appellant would further note that creating solder balls with the claimed diameter of less than 100 microns is not an obvious matter. Appellant has discovered a specific way of doing this using a tape liftoff process. See pages 7 – 8 of the specification. There is absolutely no evidence in the record to show that one of ordinary skill in the art, at the time of the present invention, knew how to make such small solder contacts as required by In re Hoeksema and its progeny, discussed above. Furthermore, Appellant disagrees with the Office Action pronouncement that "[t]he determination of parameters such as size/dimension, range and shape of the metal/solder contacts ... is a subject of routine experimentation and optimization ... ."

See Office Action, page 5. At the time of the present invention, there was no known way to experiment or optimize to attain solder balls with a diameter of less than 100 microns. There having been no known method for forming solder balls having a diameter of less than 100 micron, it is inaccurate to say that experimentation to achieve such small solder contacts would have been routine. Accordingly, for the reasons given, the rejections of claims 40, 45-51, 68, and 71 should be reversed.

B. The Subject Matter of Claims 74-75 Would Not Have Been Obvious Over Yamamoto in View of Svetkoff

Claims 74-75 depend from claim 40 and are allowable over Yamamoto taken with Svetkoff for the reasons claim 40 is allowable, discussed in Part A above. Accordingly, for this reason alone, the rejection of claims 74 and 75 should be reversed. Additionally, claims 74-75 stand on their own because they are directed to semiconductor devices having solder contacts with a diameter of less than 50 microns and less than 25 microns, respectively. Should the Board determine that claim 40 reciting solder balls having a diameter of "less than 100 microns" is obvious, Appellant submits that the semiconductor devices of claims 74-75 (utilizing even smaller solder balls) would still not have been obvious and therefore should be allowed on that separate basis. As explained above, semiconductor devices utilizing on-die solder contacts with a diameter of less than 100 microns were not known in the art, and represent a significant development in the field. The semiconductor devices of claims 74 and 75 include solder contacts of less than 50 microns or less than 25 microns, respectively, which is significantly smaller than even the less than 100-micron solder balls recited in claim 40. Semiconductor devices with such small solder contacts are a correspondingly greater departure from the prior art and achieving these semiconductor devices presented a commensurately greater challenge. Therefore, claims 74 and 75 should be recognized as non-obvious in view of the prior art, even if claims directed to semiconductor devices with on-die solder contacts having a diameter

of "less that 100 microns" are deemed obvious. Accordingly, the rejection of claims 74 and 75 should be reversed.

C. The Subject Matter of Claim 43 Would Not Have Been Obvious Over Yamamoto in View of Svetkoff

Claim 43 recites the semiconductor device of claim 40 wherein the "solder contacts have a diameter less than 10 microns." Claim 43 depends from claim 40 and is allowable over Yamamoto taken with Svetkoff for the reasons claim 40 is allowable, discussed in Part A above. If the Board finds that claim 40 reciting solder balls with a diameter of "less than 100 microns" is obvious, nonetheless, Appellant submits that the semiconductor device of claim 43 (utilizing solder balls of less than 10 microns) would still not have been obvious and therefore should be allowed on that separate basis. Before the Appellant disclosed a method of forming the semiconductor devices of the present invention, semiconductor devices having such small on-die solder balls were unknown in the prior art. Indeed, the semiconductor device of claim 43 includes an on-die solder contact of 10 μm, which is at least an order of magnitude smaller than the largest size recited in claim 40. Semiconductor devices having such small solder balls were a heretofore unattainable achievement in the art. Accordingly, claim 43 should stand as non-obvious in view of the prior art, and the rejection thereof should be reversed.

Even if the Board determines that Yamamoto and Svetkoff are properly combinable and that Svetkoff does contain an enabling disclosure of solder contacts having a diameter of 10-300 μm, claim 43 must stand regardless because it recites solder contacts with a diameter outside the disclosed range, i.e., having a diameter less than 10 μm.

D. The Subject Matter of Claims 44 and 72 Would Not Have Been Obvious Over Yamamoto in View of Svetkoff

Claims 44 and 72 recite the semiconductor device of claim 40 wherein the solder contacts have a diameter of approximately 2 microns. Claims 44 and 72 are allowable over Yamamoto taken with Svetkoff for the reasons claim 40 is allowable, discussed in Part A above. Even if the Board determines that Yamamoto and Svetkoff are properly combinable and that Svetkoff does contain an enabling disclosure of solder contacts having a diameter of 10-300 μm, claims 44 and 72 must stand regardless because they recite solder contacts with a diameter significantly outside the disclosed range, i.e., having a diameter of approximately 2 μm. Appellant has consistently explained that the semiconductor device of the present invention having on-die solder contacts with a diameter of "less than 100 microns" was unknown in the art before Appellant provided a method for forming such small solder balls. The same is true of the semiconductor devices of claims 44 and 72, but to a significantly greater degree. Not only are the 2-micron solder contacts provided in claims 44 and 72 smaller than those previously known in the art by significantly more than an order of magnitude, solder contacts of this size have not been disclosed at all by any reference. Claims 44 and 72 therefore should not be deemed obvious in view of the prior art, and the rejection of these claims should be reversed.

E. The Subject Matter of Claim 69 Would Not Have Been Obvious Over Yamamoto and Svetkoff in View of Wojnarowski

Claim 69 is allowable over Yamamoto and Svetkoff taken with Wojnarowski for the reasons claim 40 is allowable, discussed in Part A above. Additionally, claim 69 recites the semiconductor device of claim 40 wherein the "metal pad comprises a metal stack comprising four different metal levels." The January 15, 2004 Office Action correctly states that "Yamamoto and Svetkoff et al. fail to teach the metal pad comprising a stack comprising four different metal levels." See Office Action, page 9.

The Office Action states that Wojnarowski discloses this missing limitation. Appellant respectfully disagrees with the Office Action's interpretation of Wojnarowski.

The Office Action states: "Wojnarowski teaches a device having a pad metallization comprising four or more metal layers/levels comprising an aluminum (40 in Fig. 5-8; Col. 6, line 41), chromium, titanium or nickel-titanium (Col. 7, line 41) and one or more layers/levels of different metals including gold, copper, platinum, etc. (Col. 7, lines 43-46) to provide and improved adhesion and diffusion barrier (Col. 7, lines 36-46)." See Office Action, page 9. Contrary to the Office Action's assertion, these various elements disclosed in Wojnarowski do not amount to a "metal pad [comprising] a metal stack comprising four different metal levels," as recited in Claim 69 of the present invention.

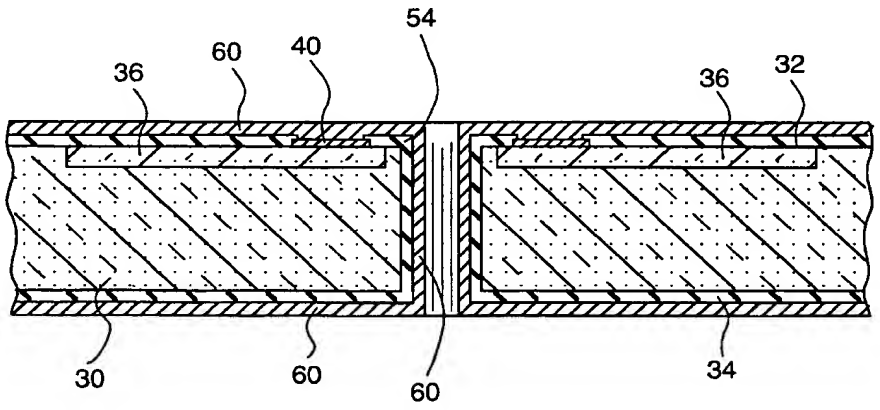


FIG. 5

Referring to Wojnarowski Fig. 5, reproduced above, semiconductor wafer 30 includes active device region 36 having top interconnection pads 40, which "are typically aluminum." See specification at col. 6, lines 38-40. According to Wojnarowski, wafer 30, with access to pad 40 open, is "metallized on both sides, forming metallization 60" in contact with pad 40. See specification at col. 7, lines 38-46.

This metallization includes a first "adhesion promotion and barrier layer," and a second "conducting metal layer of one or more difference metals which is several microns thick." Id.

Thereafter, Wojnarowski discloses patterning a resist over metallization 60 to remove all excess metal and form a patterned metal 62, as shown in Fig. 8, reproduced below. See specification at col. 7, lines 47-53. Patterned metal 62 is the conduit by which "top wafer pads 40 are electrically relocated to metal pads 64 on the bottom 34 of wafer 30." Id.

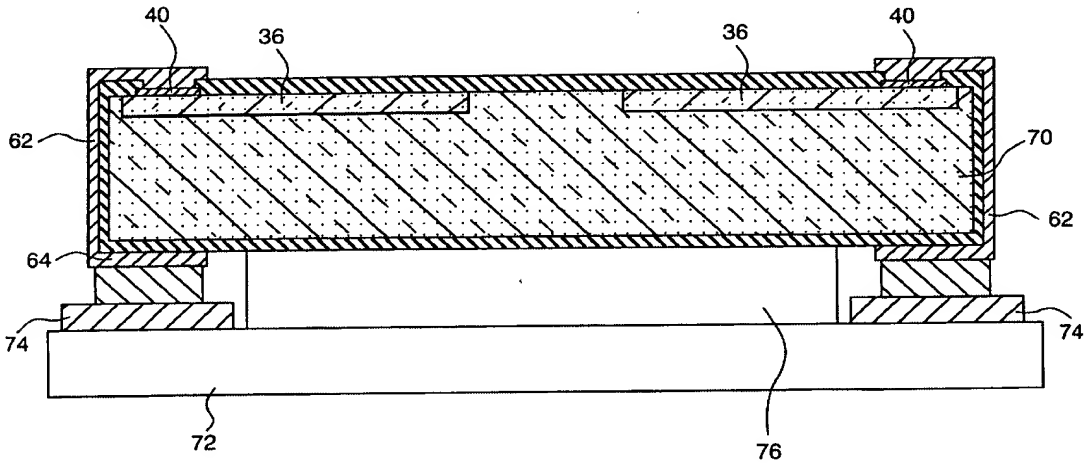


FIG. 8

Appellant submits that Wojnarowski does not disclose a "metal pad compris[ing] a metal stack comprising four different metal levels," as recited in claim 69. Rather, Wojnarowski discloses a metal pad 40 having only one metal level, adjacent to a separate and distinct "patterned metal" 62 formed from a "metallization" 60. Patterned metal 62 is not a metal stack with four metal levels for conducting an electric charge from a metal pad to a solder contact, as in claim 69, but rather a metallization with a single barrier layer (col. 7, line 41-42), and a single "conducting metal layer" (col.

7, line 43) for "electrically relocating" interconnection pad 40 to bottom pad 64, which is formed from the same metallization as patterned metal 62.

Even if metal pad 40 and patterned metal 62 are characterized as a stack in accordance with claim 69, Wojnarowski discloses at most three (not four) levels: interconnection pad 40, and the single barrier layer and single conducting metal layer which make up patterned metal 62. Although the Office Action states that Wojnarowski discloses "one or more layers/levels of different metals" in addition to interconnection pad 40 and the barrier layer, Wojnarowski actually discloses "a conducting metal layer of one or more different metals." However many different metals are alloyed or applied, Wojnarowski unambiguously includes just a single conducting metal layer. See col. 7, lines 43-44. The failure of Wojnarowski to disclose a metal pad comprising a metal stack of four metal levels is a separate and distinct reason why the rejection of claim 69 should be reversed.

F. The Subject Matter of Claim 70 Would Not Have Been Obvious Over Yamamoto Taken With Svetkoff and Wojnarowski as Applied to Claims 40 and 69 and in Further View of Takashi

Claim 70 depends from claim 69 and is allowable over Yamamoto taken with Svetkoff and Wojnarowski and in further view of Takashi for the reasons claim 69 is allowable, discussed in Part A above.

Claim 70 recites the semiconductor device of claim 69 "wherein said metal levels comprise Zirconium, Nickel, Copper and Gold." Citing the English-translation abstract of Takashi, the January 15, 2004 Office Action states that the specific metal levels recited in claim 70 would have been obvious because "Takashi et al. teach using metal pad/conductor (114 in Fig. 1-4) comprising metal such as copper and zirconium (see abstract in English Translation)." See Office Action, page 8. In fact, the Takashi abstract states, "[t]he conductors 112 and pad 114 are formed of pure copper [or] a

copper alloy, such as a copper-titanium alloy, copper-zirconium alloy, etc." See Takashi English abstract. In the metal stack recited in claim 70, zirconium and copper are not applied as a copper-zirconium alloy, but rather as a layered stack. See claims 69, 70. Takashi does not disclose use of zirconium when not alloyed with copper. Since Takashi does not teach or suggest a four layer stack of zirconium, nickel, copper, and gold, the subject matter of claim 70 is not shown or suggested by this reference. This is a separate and distinct reason why the rejection of claim 70 should be reversed.

IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

CONCLUSION

For at least the foregoing reasons, the rejections are not based on factual findings supported by "substantial evidence" as required by the Federal Circuit. See, e.g., In re Kotzab, 217 F.3d 1365, 1369 (Fed. Cir. 2000). Appellant respectfully requests this honorable Board to reverse all the rejections on appeal.

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Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/638,026.

40. (Twice amended) A semiconductor device comprising:

a semiconductor structure having at least one metal contact formed on a surface thereof;

a first insulator layer overlying said at least one metal contact;

at least one metal pad overlying said first insulator layer and in contact with said at least one metal contact;

a second insulator layer overlying said at least first one metal pad; and,

at least one solder contact formed in the second insulator and in contact with said at least one metal pad, said solder contact having a diameter less than 100 microns.

43. The semiconductor device of claim 40, wherein the solder contacts have a diameter less than 10 microns.

44. The semiconductor device of claim 40, wherein the solder contacts have a diameter of approximately 2 microns.

45. The semiconductor device of claim 40, wherein said at least one metal contact is connected to said at least one metal pad by a via hole formed in the first insulator.

46. The semiconductor device of claim 40, wherein the at least one solder contact extends from a top surface of the second insulator to the metal pad by a through hole formed in the second insulator.

47. The semiconductor device of claim 40, wherein the at least one metal pad lies at least partially overtop of the at least one metal contact.

48. The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit chip.

49. The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit wafer.

50. The semiconductor device of claim 40, wherein the semiconductor device is bonded to a module substrate.

51. The semiconductor device of claim 40, wherein the semiconductor device is bonded to a circuit board.

68. The semiconductor device of claim 40, wherein said first insulator layer is at least 2 microns thicker than said at least one metal contact.

69. The semiconductor device of claim 40, wherein said metal pad comprises a metal stack comprising four different metal levels.

70. The semiconductor device of claim 69, wherein said metal levels comprise Zirconium, Nickel, Copper and Gold.

71. (Twice amended) A semiconductor device formed on a semiconductor substrate having at least one metal contact formed thereon, said semiconductor device comprising:

a first insulator layer overlying said at least one metal contact;

at least one metal pad overlying said first insulator layer and in contact with said at least one metal contact;

a second insulator layer overlying said at least first one metal pad; and

at least one solder contact formed in the second insulator and in contact

with said at least one metal pad, said solder contact having a diameter between 2 and 100 microns.

72. The semiconductor device of claim 71, wherein said at least one solder contact has a diameter of approximately 2 microns.

74: The semiconductor device of claim 40 wherein the solder contacts have a diameter less than 50 microns.

75. The semiconductor device of claim 40 wherein the solder contacts have a diameter less than 25 microns.